D 13238 **(Pages : 2)** **Name**

Reg. No. . . . . .

FIRST SEMESTER M.Sc. DEGREE EXAMINATION, DECEMBER 2016

(CUCSS)

Computer Science

CSS 1C 05—COMPUTER ORGANIZATION AND ARCHITECTURE

(2014 Admissions)

Time : Three Hours Maximum : 36 Weightage

Part A

Answer **all** *questions.*

1. Explain any *one* error detection code.
2. Give 8-bit 2's complement and sign and magnitude representation of the following numbers : +68, —76.
3. Give block diagram of a 4 to 1 multiplexer.
4. How does a decoder works ?
5. What do you mean by addressing mode ?
6. Define "Instruction cycle".
7. Give block diagram of array multiplier.
8. Differentiate between restoring and non-restoring algorithms for division.
9. What do you mean by memory interleaving ?
10. Differentiate between SRAM and DRAM.What are the different types of DRAMs.
11. List and explain any *two* 8085 data movement instructions, one direct and one indirect addressing mode.
12. List and state functions of 8085 flags.

(12 x 1 = 12 weightage)

Part B

Answer any six *questions.*

13. With the help of a block diagram, explain the working of bi-directional shift register.
14. Simplify the following function using K-map and implement with AND-OR gates :

$f = X3\ X4 + X1\ \overline{X3}\ X4 + X2\ X4 + X1\ X4.$

Turn over

15. Discuss the classification of instructions based on function. Explain the execution of a branch instruction.

16. Explain single bus, two bus and three bus organization.

17. Explain floating point number representation.

18. Explain interrupt driven JO. Discuss interrupt nesting.

19. With suitable example, explain typical organization of 256K DRAM.

20. Draw and explain timing diagram for 'MVI A, data' instruction (8085).

21. Discuss 8051 interrupts.

(6 x 2 = 12 weightage)

Part C

Answer any **three** *questions.*

22. (i) What are the different types of counters. Explain 4-bit ripple counter.

(ii) Give the excitation table, block diagram and working of JK and D flip flops.

23. (i) Explain register transfer language with suitable examples.

(ii) Explain basic principle and working of DMA.

24. Give a detailed account of microprogrammed and hardwired control units.

25. Explain Booth algorithm. Multiply —23 and +56 (assume 8-bit representation) using Booth algorithm. Discuss how bit pair recoding speeds up multiplication.

26. Explain basic principle and working of cache memory. Differentiate between level I and Level II cache memory. Explain Associative and set associative cache mapping techniques.

27. Discuss architecture of 8086 processor.

(3 x 4 = 12 weightage)